CAMAC Quad Ramp Controller
(CAMAC Module C473)

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General Description

The C473 is a programmable ramp controller capable of generating four semi-independent, time-based analog outputs. These outputs are updated at a 100 kHz rate.

The C473 also contains digital control capabilities to turn on, turn off, and reset four power supplies. It can also return eight status bits, a ramp enable bit, a power supply enable bit, and a power supply interlock bit from each of the regulator supplies.

Features

Output Functions

The ramp outputs will have the form:

output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The output functions of all four channels share a common trigger. There is a delay, programmable from 0 to 255 μsec, between the TCLK trigger event and the start of the output functions. The output functions of all four channels will begin simultaneously following the delay.

Note: Although the shortest programmable delay is 0 μsec, at least 30 μsec must be allowed for the processor to service the trigger interrupt. No mechanism is in place in the C473 to enforce a minimum programmed delay.

Scale Factors

Scale factors are 16 bits long. The upper byte is interpreted as the whole number part and the lower byte is interpreted as the fractional part of the scale factor. Positive and negative scale factors are allowed. The largest negative scale factor is -128.000. The largest positive scale factor is approximately 127.996.

A separate scale factor is programmed for each interrupt level for each channel.

Changes to active scale factors are updated at the start of the next ramp.

Offsets

Offsets are 16 bits long. Positive and negative offsets are allowed. The largest negative scale factor is -32768. The largest positive scale factor is 32767.

A separate offset is programmed for each interrupt level for each channel.

Changes to active offsets are updated at the start of the next ramp.

Overflow Errors

The FPGA checks for overflow errors following each calculation and maintains the previously calculated value if an overflow is detected.

Ramp Output

The outputs are provided in analog format (16 bits, +/- 10.000V).

Bias Input

An analog input is supplied that will accept a +/- 5V input. The voltage is not monitored or processed by the C473's FPGA or firmware. This signal will be doubled and analog-added to each channel's ramp output.

ADC Monitoring

Each channel's final output (after adding the Bias Input) is constantly compared to a voltage feedback signal from that channel's power supply. This is accomplished by applying the final output and feedback input to the inputs of a differential instrumentation amplifier. The output of this amplifier is monitored by the FPGA through an ADC and compared to a programmable error threshold value.

Tables

The overall shape of the output function is defined by f(t). Each f(t) is programmed into a table in the C473 as a piecewise linear curve. Each channel will have sixteen possible tables with a maximum of 64 points each. Each point consists of a ramp value V and a delta-t value. The last delta-t value of each table must be zero. At the end of each function, the final value will be held.

Table selection is effected by an interrupt. Twenty-six interrupt levels are available. Each is asserted by the 'or' of up to 256 programmed TCLK events. It is impossible to program one given TCLK event to trigger multiple interrupt levels at the same time. Programming a given TCLK event to trigger a second interrupt level will overwrite the first. Interrupt levels can also be asserted via an F(17)A(10) CAMAC command. The complete list of TCLK events can be found in the TCLK Event Definitions document.

The FPGA constantly monitors the TCLK input. When a TCLK event is detected that is programmed to trigger an interrupt level, the FPGA will interrupt the processor and start a delay timer. The processor reads from the FPGA which interrupt level has begun, and downloads to the FPGA a scale factor, offset, and ramp table for each channel. At the end of the programmable delay, the FPGA will begin generating the output function.

Note: The FPGA will begin generating the output function after the delay, regardless of whether or not the processor has completed the parameter download. A very short delay may not allow

the processor enough time to complete the download and may result in unexpected operation. **A minimum delay of 30 μsec is recommended.**

Tables are selected via pointers with values of 0 to 15 indicating ramp numbers 0 through 15.

Changes to an active table are implemented at the start of the next ramp. Changes to table pointers are updated at the start of the next ramp.

Initialized State

When the C473 is powered up or reset, all scale factors will be set to unity (0x0100). All table pointers will be set to zero, and all table values will be set to zero. The clock event table will be filled with zeros, which will clear all "valid entry" bits.

CAMAC Functions

It should be noted that this section uses CAMAC notation when describing data bits. CAMAC data bits are R16:R1 for reads and W16:W1 for writes, with R16 and W16 being most significant. The most significant bytes are R16:R9 and W16:W9. The least significant bytes are R8:R1 and W8:W1.

F(0)A(0) – Read f(t) table data

F(t) data will be returned in f(t), delta-t order, starting at the point defined with a write to F(16)A(12). Data is read directly out of processor memory. The channel number, table number, and table entry number written to F(16)A(12) set the memory pointer as follows:

```
ptr = Channel * 16 * 64 * 2 +
            Table# * 64 * 2 +
            Table Entry * 2
```

The data pointer is auto-incremented with each successive call to F(0)A(0). When the end of one ramp is reached, successive reads will return data for the next ramp. When the end of one channel's ramps is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

F(0)A(0)

Bits	Bit Definitions
R16:R1	F(t) table data

F(0)A(5) – Read ramp table map data

Ramp table map data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(5). When the end of one channel's ramp table map is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(5) indicates the number of the ramp profile that will be used when this interrupt level is triggered.

F(0)A(5)

Bits	Bit Definitions
R16:R5	Reserved
R4:R1	Ramp Profile Number (0-15)

F(0)A(6) – Read delay data

Ramp delay data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The entry number written to F(16)A(13) sets the memory pointer as follows:

```
ptr = Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(6). After data for interrupt level 25 is read, the next read will return data for interrupt level 0.

The value returned by F(0)A(6) indicates the length of the delay that will be used when this interrupt level is triggered.

F(0)A(6)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Ramp Delay (0-255 microseconds)

F(0)A(7) – Read offset data

Offset data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(7). When the end of one channel's offset data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(7) is the offset that will be used when this interrupt level is triggered.

F(0)A(7)

Bits	Bit Definitions
R16:R1	Offset (-32768 – +32767)

F(0)A(8) – Read scale factor data

Scale factor data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(8). When the end of one channel's scale factor data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(8) is the scale factor that will be used when this interrupt level is triggered. See the section on Scale Factors for an explanation of how scale factor data is interpreted.

F(0)A(8)

Bits	Bit Definitions
R16:R1	Scale factor (-128.0 – 127.9)

F(0)A(9) – Read TCLK trigger map data

TCLK trigger map data will be returned, starting at the point defined with a write to F(16)A(11). Data is read directly out of processor memory. The TCLK event written to F(16)A(11) sets the memory pointer as follows:

```
ptr = TCLK event
```

If bit R8 is set, the rest of the value returned indicates which interrupt level will be triggered by this TCLK event. If R8 is cleared, this TCLK event will not trigger any interrupt level.

The data pointer is auto-incremented with each successive call to F(0)A(9). After data for TCLK $FF is read, the next read will return data for TCLK $00.

F(0)A(9)

Bits	Bit Definitions
R16:R9	Reserved
R8	Valid Entry 1 = This TCLK event will trigger the interrupt level in R5:R1 0 = This TCLK event will not trigger an interrupt level
R7:R6	Reserved
R5:R1	Interrupt Level

F(1)A(2) – Read most recent DAC setting

The most recent DAC setting will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(2). After Channel 3 is read, the next read will return data for Channel 0.

F(1)A(2)

Bits	Bit Definitions
R16:R1	DAC setting (-32768 – +32767)

F(1)A(7) – Read power supply status nominal

The nominal power supply status will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(7). After Channel 3 is read, the next read will return data for Channel 0.

This is the value "expected" to be returned by a read of power supply status.

F(1)A(7)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset (1 = Reset output active)
R13	Ramp Active
R12	Interlock Input (1 = Interlock input active)
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs

F(1)A(8) – Read power supply status mask

The power supply status mask will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(8). After Channel 3 is read, the next read will return data for Channel 0.

A bit cleared in the status mask will suppress errors when the actual power supply status bit does not match the nominal status bit.

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F(1)A(8)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset
R13	Ramp Active
R12	Interlock Input
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs

F(1)A(9) – Read LAM mask

The CAMAC Look-At-Me (LAM) mask will be returned.

A bit cleared in the LAM mask will suppress LAM when the corresponding bit is set in the LAM Source.

Deleted: set

F(1)A(9)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	External Permit (Interlock)
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(1)A(11) – Read and clear power supply status error

The power supply status error register will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(11). After Channel 3 is read, the next read will return data for Channel 0.

A bit set in the status error register indicates the value of that bit in the power supply status register(F(4)A(1)) did not match that bit in the power supply status nominal register(F(1)A(7)), and that bit was not cleared in the power supply status mask register(F(1)A(9)). Mismatches are latched into the error register.

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Reading F(1)A(11) clears the power supply error register.

F(1)A(11)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset
R13	Ramp Active
R12	Interlock Input
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs

F(1)A(12) – Read and clear LAM source register

The CAMAC Look-At-Me (LAM) source register will be returned and cleared.

F(1)A(12)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	External Permit (Interlock)
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(1)A(13) – Read most recent CAMAC command

The most recent CAMAC command is returned.

F(1)A(13)

Bits	Bit Definitions
R16:R9	Function
R8:R1	Subaddress

F(2)A(0) – Read TCLK interrupt level count

Returns the number of times a particular interrupt level has been triggered. First select a particular interrupt level with F(17)A(0).

F(2)A(0)

Bits	Bit Definitions
R16:R1	Interrupt Level Count

F(2)A(9) – Read time remaining in current ramp segment

The number of samples remaining in the current ramp segment is returned. First select a channel with F(19)A(1).

F(2)A(9)

Bits	Bit Definitions
R16:R1	Sample Count Remaining

F(3)A(14) – Read 1Hz interrupt count

A counter in the C473 increments once per second. Returns the number of 1Hz interrupts.

F(3)A(14)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Count

F(3)A(15) – Read CAMAC interrupt count

A counter in the C473 increments once every time the CAMAC service routine is entered. Returns the number of CAMAC interrupts.

F(3)A(15)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Count

F(4)A(1) – Read power supply status

The power supply status will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(4)A(1). After Channel 3 is read, the next read will return data for Channel 0.

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F(4)A(1)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset (1 = Reset output active)
R13	Ramp Active
R12	Interlock Input (1 = Interlock input active)
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs

F(4)A(3) – Read power supply tracking tolerance

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The power supply tracking tolerance is returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(4)A(3). After Channel 3 is read, the next read will return data for Channel 0.

The voltage difference between channel output (after analog summer) and power supply feedback is constantly monitored. If the magnitude (absolute value) of the error exceeds the tolerance for 16 consecutive samples, a power supply tracking error is declared.

F(4)A(3)

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Bits	Bit Definitions
R16:R1	Tolerance (0 – +32767)

F(4)A(12) – Read, but do not clear, LAM source register

The CAMAC Look-At-Me (LAM) source register will be returned, but not cleared.

F(4)A(12)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	External Permit (Interlock)
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(5)A(0) – Read ADC

The ADC value will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(2). After Channel 3 is read, the next read will return data for Channel 0.

This reading is the voltage difference between the card output (after analog summer) and the power supply feedback signal.

F(5)A(0)

Bits	Bit Definitions
R16:R1	ADC reading (-32768 – +32767)

F(6)A(0) – Read module ID number

F(6)A(0)

Bits	Bit Definitions
R16:R1	0x01D9 (473)

F(6)A(1) – Read firmware version number

F(6)A(1)

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision

F(6)A(2) – Read a word in memory

Return a word in memory from an address defined by writing to F16A14.

F(6)A(2)

Bits	Bit Definitions
R16:R1	Memory Data

F(6)A(3) – Read a block memory

Return a word in memory from an address defined by writing to F16A14. The address is auto-incremented with each successive read from F(6)A(3).

F(6)A(3)

Bits	Bit Definitions
R16:R1	Memory Data

F(6)A(4) – Read diagnostic counter

Returns diagnostic counter data. Which counter is selected by F(19)A(2).

F(6)A(4)

Bits	Bit Definitions
R16:R1	Count

F(6)A(8) – Read FPGA version number

F(6)A(8)

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision

F(8)A(0) – Read LAM status

F(8)A(0)

Bits	Bit Definitions
R16:R2	Reserved
R1	LAM status

F(9)A(0) – Reset module

The C473 will be reset. This function is handled by hardware.

F(16)A(0) – Write f(t) table data

F(t) data will be written in f(t), delta-t order, starting at the point defined with a write to F(16)A(12). Data is entered directly into processor memory. The channel number, table number, and table entry number written to F(16)A(12) set the memory pointer as follows:

```
ptr = Channel * 16 * 64 * 2 +
            Table# * 64 * 2 +
            Table Entry * 2
```

The data pointer is auto-incremented with each successive call to F(16)A(0). When the end of one ramp is reached, successive calls will write data for the next ramp. When the end of one channel's ramps is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

F(16)A(0)

Bits	Bit Definitions
W16:W1	F(t) table data

F(16)A(5) – Write ramp table map data

Ramp table map data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(5). When the end of one channel's ramp table map is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(16)A(5) indicates the number of the ramp profile that will be used when this interrupt level is triggered.

F(16)A(5)

Bits	Bit Definitions
W16:W5	Reserved
W4:W1	Ramp Profile Number (0-15)

F(16)A(6) – Write delay data

Ramp delay data will be written, starting at the point defined with a write to F(16)A(13). Data is read directly into processor memory. The entry number written to F(16)A(13) sets the memory pointer as follows:

```
ptr = Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(6). After data for interrupt level 25 is written, the next call will write data for interrupt level 0.

The value written by F(16)A(6) indicates the length of the delay that will be used when this interrupt level is triggered.

F(16)A(6)

Bits	Bit Definitions
W16:W9	Reserved
W8:W1	Ramp Delay (0-255 microseconds)

F(16)A(7) – Write offset data

Offset data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(7). When the end of one channel's offset data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(16)A(7) is the offset that will be used when this interrupt level is triggered.

F(16)A(7)

Bits	Bit Definitions
W16:W1	Offset (-32768 – +32767)

F(16)A(8) – Write scale factor data

Scale factor data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 26 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(8). When the end of one channel's scale factor data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(16)A(8) is the scale factor that will be used when this interrupt level is triggered. See the section on Scale Factors for an explanation of how scale factor data is interpreted.

F(16)A(8)

Bits	Bit Definitions
W16:W1	Scale factor (-128.0 – 127.9)

F(16)A(9) – Write TCLK trigger map data

TCLK trigger map data will be written, starting at the point defined with a write to F(16)A(11). Data is written directly into processor memory. The TCLK event written to F(16)A(11) sets the memory pointer as follows:

```
ptr = TCLK event
```

If bit R8 is set, the rest of the value written indicates which interrupt level will be triggered by this TCLK event. If R8 is cleared, this TCLK event will not trigger any interrupt level.

The data pointer is auto-incremented with each successive call to F(16)A(9). After data for TCLK $FF is written, the next call will write data for TCLK $00.

F(16)A(9)

Bits	Bit Definitions
W16:W9	Reserved
W8	Valid Entry 1 = This TCLK event will trigger the interrupt level in W5:W1 0 = This TCLK event will not trigger an interrupt level
W7:W6	Reserved
W5:W1	Interrupt Level

F(16)A(11) – Set up TCLK trigger map pointer

The TCLK trigger map pointer will be written. The pointer is a TCLK event. Data written to this memory location defines the interrupt level that the TCLK event will trigger.

F(16)A(11)

Bits	Bit Definitions
W16:W9	Reserved
W8:W1	TCLK trigger map pointer (TCLK event)

F(16)A(12) – Set up pointer for ramp data read/write

F(16)A(12)

Bits	Bit Definitions
W16:W11	Table Entry #
W10:W6	Table #
W5:W3	Reserved
W2:W1	Channel #

F(16)A(13) – Set up pointer for map, scale factor, offset, and delay read/write

F(16)A(13)

Bits	Bit Definitions
W16:W11	Reserved
W10:W6	Entry #
W5:W3	Data Type 0 = Ramp Table Map 1 = Delay 3 = Scale Factor 4 = Offset
W2:W1	Channel #

F(16)A(14) – Set up diagnostic memory pointer

Two successive writes to F(16)A(14) define the 32-bit Diagnostic Memory Pointer. The first write will define the lower (least significant) 16 bits. The second write will define the upper (most significant) 16 bits.

F(16)A(14)

Bits	Bit Definitions
W16:W1	Diagnostic memory pointer

F(17)A(0) – Write TCLK Interrupt Level Counter Pointer

F(17)A(0)

Bits	Bit Definitions
W16:W1	TCLK Interrupt Level Counter Pointer

F(17)A(2) – Write directly to DAC

Write directly to the DAC for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(2). After Channel 3 is written, the next call will write data for Channel 0.

F(17)A(2)

Bits	Bit Definitions
W16:W1	DAC setting (-32768 – +32767)

F(17)A(7) – Write power supply status nominal

The nominal power supply status will be written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(7). After Channel 3 is written, the next call will write data for Channel 0.

This is the value "expected" to be returned by a read of power supply status.

F(17)A(7)

Bits	Bit Definitions
W16	Reserved
W15	Power Supply Tracking Error
W14	Power Supply Reset (1 = Reset output active)
W13	Ramp Active
W12	Interlock Input (1 = Interlock input active)
W11	Power Supply Enabled
W10	Overflow
W9	Ramp Enabled
W8:W1	State of power supply status inputs

F(17)A(8) – Write power supply status mask

The power supply status mask will be written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(8). After Channel 3 is written, the next call will write data for Channel 0.

A bit cleared in the status mask will suppress errors when the actual power supply status bit does not match the nominal status bit.

Deleted: set

F(17)A(8)

Bits	Bit Definitions
W16	Reserved
W15	Power Supply Tracking Error
W14	Power Supply Reset
W13	Ramp Active
W12	Interlock Input
W11	Power Supply Enabled
W10	Overflow
W9	Ramp Enabled
W8:W1	State of power supply status inputs

F(17)A(9) – Write LAM Mask

The CAMAC Look-At-Me (LAM) mask will be written.

A bit cleared in the LAM mask will suppress LAM when the corresponding bit is set in the LAM Source.

Deleted: set

F(17)A(9)

Bits	Bit Definitions
W16	CAMAC Command Error
W15	Calculation Error (Overflow)
W14	Unused
W13	TCLK Missing
W12	Unused
W11	External Permit (Interlock)
W10	Power Supply Tracking Error
W9:W5	Unused
W4	Power Supply 3 Error
W3	Power Supply 2 Error
W2	Power Supply 1 Error
W1	Power Supply 0 Error

F(17)A(10) – Manual Interrupt Level Trigger

Manually trigger an interrupt level. Issuing this command will trigger an interrupt level, just as if a TCLK event occurred that was mapped to that interrupt level, including delay. If a ramp is active at the time this command is sent, it will be ignored, just as if a mapped TCLK event had come along while a ramp was active.

F(17)A(10)

Bits	Bit Definitions
W16:6	Reserved
W5:W1	Interrupt Level

F(19)A(1) – Write Channel Pointer

F(19)A(1)

Bits	Bit Definitions
W16:W1	Channel Pointer

F(19)A(2) – Select Diagnostic Counter

F(19)A(2)

Bits	Bit Definitions
W16:W1	Diagnostic counter selection 0 = CAMAC interrupt counter 1 = TCLK interrupt counter (increments once each time a ramp is launched) 2 = 1Hz counter

F(20)A(3) – Write power supply tracking tolerance

The power supply tracking tolerance is written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(20)A(3). After Channel 3 is written, the next call will write data for Channel 0.

The voltage difference between channel output (after analog summer) and power supply feedback is constantly monitored. If the magnitude (absolute value) of the error exceeds the tolerance for 16 consecutive samples, a power supply tracking error is declared.

F(20)A(3)

Bits	Bit Definitions
W16:W1	Tolerance (0 – +32767)

F(24)A(3) – Disable LAM

CAMAC Look-At-Me (LAM) will be disabled.

All data sent with F(24)A(3) is ignored.

F(24)A(5) – Disable Channel Waveform

Disable the waveform output for the channel selected by F(19)A(1). The next TCLK trigger will result in no waveform output for this channel. The last value written to the DAC will be held. Manual DAC writes will still have effect. The channel number is auto-incremented with each successive call to F(24)A(5). After Channel 3, the next call will disable Channel 0.

All data sent with F(24)A(5) is ignored.

F(24)A(6) – Turn off power supply

Turn off the power supply for the channel selected by F(19)A(1). The power supply will immediately be turned off. The channel number is auto-incremented with each successive call to F(24)A(6). After Channel 3, the next call will turn off Channel 0.

All data sent with F(24)A(6) is ignored.

F(25)A(0) – Decrement the DAC

Decrement the DAC for the channel selected by F(19)A(1). If the DAC is already at -32768, this command will be ignored.

Unlike most other commands, the channel number will not be auto-incremented with each successive call to F(25)A(0) or F(25)A(1), allowing one channel's DAC to be incremented or decremented several times in a row without resetting the channel number.

All data sent with F(25)A(0) is ignored.

F(25)A(1) – Increment the DAC

Increment the DAC for the channel selected by F(19)A(1). If the DAC is already at +32767, this command will be ignored.

Unlike most other commands, the channel number will not be auto-incremented with each successive call to F(25)A(0) or F(25)A(1), allowing one channel's DAC to be incremented or decremented several times in a row without resetting the channel number.

All data sent with F(25)A(1) is ignored.

F(26)A(3) – Enable LAM

CAMAC Look-At-Me (LAM) will be Enabled.

All data sent with F(26)A(3) is ignored.

F(26)A(5) – Enable Channel Waveform

Enable the waveform output for the channel selected by F(19)A(1). The next TCLK trigger will result in normal waveform output for this channel. The channel number is auto-incremented with each successive call to F(26)A(5). After Channel 3, the next call will enable Channel 0.

All data sent with F(26)A(5) is ignored.

F(26)A(6) – Turn on power supply

Turn on the power supply for the channel selected by F(19)A(1). The power supply will immediately be turned on if the interlock input is active. The channel number is auto-incremented with each successive call to F(26)A(6). After Channel 3, the next call will turn on Channel 0.

All data sent with F(26)A(6) is ignored.

F(26)A(8) – Reset power supply

Reset the power supply for the channel selected by F(19)A(1). The power supply's reset signal will be activated for one second. The channel number is auto-incremented with each successive call to F(26)A(8). After Channel 3, the next call will turn on Channel 0.

All data sent with F(26)A(8) is ignored.

Theory of Operation

Ramp Outputs

The C473 user programs the card with the following data:

- Which TCLK events will cause triggers
- Which interrupt levels will activate as a result of TCLK event triggers. Each TCLK event will trigger either zero or one interrupt level, never more than one. Every channel will execute the same interrupt level, but each channel will have its own ramp profile, scale factor, and offset.
- Delay between TCLK event and start of ramp outputs. All four ramp outputs will start simultaneously.
- A table of ramp profiles (the basic shape of the ramp output). Each channel gets its own table of ramp profiles.
- Which ramp profile to use by each channel for each interrupt level
- A scale factor to use for each interrupt level. Each channel will have a unique scale factor.
- An offset to use for each interrupt level. Each channel will have a unique offset.

The C473 constantly monitors TCLK. Every time a TCLK event is received, the FPGA uses that event as an address to read a RAM containing interrupt level map data. Bit 7 of this data will have been set if this TCLK event is enabled to cause a trigger. Bits 4:0 indicate which interrupt level will be triggered.

If an enabled TCLK event is detected, and none of the ramp outputs are already running (RAMP_ACTIVE output from RAMP_CTRL module), the FPGA will interrupt the processor. Simultaneously, the FPGA will use the decoded interrupt level as an address to another RAM containing delay data and preset a counter with this data. The counter decrements once every microsecond.

Once interrupted, the processor must very quickly start downloading ramp parameters to the FPGA. The scale factors, offsets, and first (f(t), delta-t) data points must be downloaded to the FPGA before the counter reaches zero. After this first set of data, the rest of the (f(t), delta-t) data points must be downloaded fast enough to stay ahead of the ramp (10 µsec per data point).

Typically, it takes about 15 µsec for the processor to download the initial data set, and 3 µsec to download each data point for four channels after that. Care must be taken not to write code that will interfere with servicing this interrupt. If other interrupts will be serviced by the processor (for timers, CAMAC communications, etc), it is highly recommended that those routines start and end with alt_irq_interruptible() and alt_irq_non_interruptible(), respectively, to allow the ramp download service routine to interrupt them.

When the counter reaches zero, the FPGA starts sending ramp data to the DAC. The FPGA does not know the difference between “old” and “new” data, “good” or “bad”. If the user has not programmed a long enough delay to allow the processor to download the new ramp, the FPGA will simply start sending data from the previous ramp.

The ramp output will take the following form:
output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The function f(t) is downloaded to the FPGA as a piecewise linear curve. Each point consists of a ramp value V (before being scaled and offset) and a delta-t value. Delta-t_n defines the number of samples (at 10 µsec per sample) between V_n and V_{n+1}.

Samples between points n and n+1 are interpolated as follows:

$$V = scale\_factor * \left(V_{n+1} - \left(\frac{(V_{n+1} - V_n)}{deltat(n)} * samples\_remaining \right) \right) + offset$$

The final delta-t value of f(t) must be zero. A delta-t of zero is the flag the FPGA uses to indicate the end of the ramp. The final V value will be held until the next ramp (or manual set, increment/decrement, etc).

The FPGA constantly monitors ramp calculations for overflows. An overflow will occur if a data point's value would be less than -32768 or greater than 32767. If an overflow is detected, the last valid value is held.

ADC Inputs

The output of the C473 (after summer) is compared to an analog feedback signal from the power supply. An error signal is created by applying these two signals to the two sides of a differential instrumentation amplifier. The error signal is read by a sixteen-bit ADC every time the DAC is loaded with new data or every 25.6 µsec (1024 clocks @ 40 MHz), whichever comes first. The digitized error signal is compared to a threshold value, programmed by the user. If the absolute value of the error is greater than the threshold value for sixteen consecutive samples, the power supply is declared "out of tolerance" and an error flag is set.

Processor I/O Memory Map

This section is intended for people who wish to write code to run in the C473. Users of the C473 may also gain greater insight into the C473's sequence of operations.

The C473's software runs on an Altera NiosII processor, embedded in the FPGA. The processor is connected to all of its peripherals automatically by Altera's SOPC Builder tool. SOPC builder automatically assigns base addresses to all of the peripherals. Adding, deleting, or modifying these peripherals usually results in completely different base addresses being assigned. These base addresses are aliased by #define's in the file system.h. System.h is automatically generated by Altera's NiosII IDE. Because the actual base addresses are constantly shifting, the system.h aliases are used in this document instead. The one device that has a locked base address is the flash memory.

1. Flash Memory
Flash memory is hard coded to a base address of 0x00000000. Memory space is reserved for as much as 16 megabytes of flash memory. The C473 board is laid out to accommodate a Spansion (AMD) AM29LV128M or equivalent. A smaller part with equivalent pinout may be substituted.

2. SRAM
Up to two megabytes of SRAM is located at EXT_SSRAM_BASE. The C473 is laid out to accommodate a Cypress CY7C1380 synchronous SRAM or equivalent. A smaller part with equivalent pinout may be substituted.

3. Timers
Three timer peripherals are included. See Chapter 12 of Altera's QuartusII Handbook Volume 5: Embedded Peripherals, "Timer Core With Avalon Interface" for programming information.

The system clock timer (SYS_CLK_TIMER_BASE) is used by the processor to generate system delays, such as when using the usleeep() function.

Two other timers are included (TIMER_1SEC_BASE and TIMER_100HZ_BASE) and are intended to be used to generate interrupts at regular 1 second and 10 msec intervals.

4. Ramp Controller (TCLK_RAMP.VHD)

The Ramp Controller is mapped to TCLK_RAMP_0_BASE. It contains the TCLK Decoder, Ramp Launch Control, the Ramp Generators, and the DAC Controller. Only the Ramp Launch Control and Ramp Generators are addressable.

4.1. Ramp Launch Control(RAMP_LAUNCH.VHD)

TCLK Trigger Map: Word32 Offset 0x0000 – 0x00FF

The TCLK Trigger Map is stored in a 256x8 SRAM in the FPGA. The Word32 offset is decoded as 0000_0000_TTTT_TTTT, where:

TTTT_TTTT = TCLK Event

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time a TCLK event is received, using the TCLK event as the read address. The FPGA determines whether or not this event is enabled for triggering, and if enabled, the FPGA will interrupt the processor, load the Active Interrupt Level register, and start a delay timer.

TCLK Trigger Map

Bits	Bit Definitions
31:8	Reserved
7	TCLK Event Enable 1 = This TCLK event is enabled to launch the interrupt level in bits 4:0 0 = This TCLK event is disabled
6:5	Reserved
4:0	Interrupt level to be launched by this TCLK event

Ramp Launch Delay: Word32 Offset 0x0100 – 0x011F

The Ramp Launch Delays are stored in a 32x8 SRAM in the FPGA. The Word32 offset is decoded as 0000_0001_000L_LLLL, where:

LLLLL = Interrupt Level

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time an enabled TCLK event is received, using the triggered interrupt level number as the read address. A delay timer is preset with this data and will decrement once every µsec. When this timer expires, the Ramp Launch Control issues the Ramp Start signal.

Ramp Launch Delay

Bits	Bit Definitions
31:8	Reserved
7:0	Ramp Launch Delay, in µsec

Active Interrupt Level: Word32 Offset 0x0200 (Read)

This register is read-only to the processor.

When the processor enters the ramp load interrupt service routine, the first thing it should do is come here and read the Active Interrupt Level register.

Active Interrupt Level

Bits	Bit Definitions
31:5	Reserved
4:0	Active Interrupt Level

IRQ Clear: Word32 Offset 0x0200 (Write)

When the processor completes the ramp load interrupt service routine, it should issue a write to this address to clear the interrupt. The simple act of writing to this register clears the interrupt. Data is ignored.

IRQ Clear

Bits	Bit Definitions
31:0	Reserved – Ignored

Manual Interrupt Level Trigger: Word32 Offset 0x0201

Writing to this register will trigger an interrupt level, just as if a TCLK event occurred that was mapped to that interrupt level, including delay. If a ramp is active at the time this command is sent, it will be ignored, just as if a mapped TCLK event had come along while a ramp was active.

This register is write-only.

Manual Ramp Trigger

Bits	Bit Definitions
31:5	Reserved
4:0	Interrupt Level

4.2. Ramp Generation (RAMP_CTRL.VHD)

Each channel has its own ramp generator. The memory map is:
Channel 0: TCLK_RAMP_0_BASE + 0x2000
Channel 1: TCLK_RAMP_0_BASE + 0x2400
Channel 2: TCLK_RAMP_0_BASE + 0x2800
Channel 3: TCLK_RAMP_0_BASE + 0x2C00

F(t) Table: Word32 Offset 0x0000 – 0x007F

F(t) data is stored in a 128x16 SRAM in the FPGA. The Word32 offset is decoded as 0000_0000_0NNN_NNNB, where:
NNNNNN = F(t) table entry number (0 – 63)
B = Voltage data or delta-t data:
0 = Voltage data V(n)
1 = delta-t data $\Delta t(n)$

This SRAM is write-only to the processor.

The Ramp Generator begins reading this SRAM after the Ramp Start signal is received from the Ramp Launch module. The Ramp Generator updates the DAC every 10 µsec until it reads zero for delta-t.

F(t) Table

Bits	Bit Definitions
31:16	Reserved
15:0	Voltage or delta-t data (-32768 – +32767)

DAC Value: Word32 Offset 0x0080

Reading this register returns the most recent value sent to the DAC.

Writing this register while the ramp is active has no effect. Otherwise, writing this register sends data to the DAC.

Note: From the processor's point of view, this data value is read and written as a signed, 16-bit value between -32768 and +32767, representing a desired voltage between -10V and +10V. The actual data sent to the DAC is translated to account for two things:

- The DAC output gets inverted by the analog summer circuit, so the actual DAC output must be "pre-inverted"
- The Burr-Brown DAC7744 used on the C473 expects a different data format: 0 to 65535 for -10V to +10V.

Anyone watching actual data transactions between the FPGA and the DAC should keep this in mind. The translation formula is:

Actual DAC Data [15] = DAC Value[15]
Actual DAC Data [14:0] = not(DAC Value[14:0])

or equivalently,

Actual DAC Data = not(DAC Value) – 0x8000

Each Ramp Generator sends its own DAC Update signal to the DAC Controller every 10 µsec during an active ramp, or in response to a manual DAC write.

DAC Value

Bits	Bit Definitions
31:16	Reserved
15:0	DAC Value (-32768 – +32767 = -10V to +10V)

Ramp/Power Supply Status: Word32 Offset 0x0081

This register returns ramp and power supply status. Writes are necessary only to clear the Overflow Status bit.

Ramp/Power Supply Status

Bits	Bit Definitions
31:14	Reserved
13	Power Supply Reset Status 1 = PS reset output active
12	Ramp Active 1 = Ramp is active
11	Power Supply Interlock Status 1 = PS Interlock input is active
10	Power Supply Enable Status 1 = PS Enable output is active
9	Overflow Status 1 = A mathematical overflow has occurred. Write 0 to this bit to clear.
8	Ramp Enabled 1 = Ramp is enabled. This is a status bit only. Writes will have no effect.
7:0	Reserved

Sample Count Remaining: Word32 Offset 0x0083

This read-only register returns the number of samples remaining in the current segment of the active F(t) piecewise-linear curve.

Sample Count Remaining

Bits	Bit Definitions
31:12	Reserved
11:0	Samples remaining

Scale Factor: Word32 Offset 0x0084

Writing this register during an active ramp will have no immediate effect. Data written here will be loaded into the Ramp Generator's scale factor register at the end of the active ramp. Writing this register while no ramp is active will immediately load the scale factor register.

Reading this register returns the scale factor register. Data may not reflect most recent write if the write occurred during an active ramp and that ramp is still active.

Scale Factor

Bits	Bit Definitions
31:16	Reserved
15:0	Scale Factor (-32768 – +32767 = -128.0 to +127.9)

Offset: Word32 Offset 0x0085

Writing this register during an active ramp will have no immediate effect. Data written here will be loaded into the Ramp Generator's offset register at the end of the active ramp. Writing this register while no ramp is active will immediately load the offset register.

Reading this register returns the offset register. Data may not reflect most recent write if the write occurred during an active ramp and that ramp is still active.

Offset

Bits	Bit Definitions
31:16	Reserved
15:0	Offset (-32768 – +32767 = -10V to +10V)

Power Supply Enable: Word32 Offset 0x0086

Writing to this register enables or disables the power supply.

This register is write-only. The power supply enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Enable 1 = Enable

Power Supply Reset: Word32 Offset 0x0087

Writing to this register sets the state of the Power Supply Reset output.

This register is write-only. The power supply reset state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Reset 1 = Reset output active

Ramp Enable: Word32 Offset 0x0088

Writing to this register enables or disables the ramp controller. Writing during an active ramp will have no immediate effect. The ramp enable bit inhibits the ramp controller's state machine from starting, but has no effect while the state machine is running.

This register is write-only. The ramp enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Ramp Enable 1 = Enable

5. ADC Controller (ADC_CTRL.VHD)

The ADC Controller is mapped to ADC_CTRL_0_BASE. The ADC data is automatically updated every time the DAC is updated or every 25.6 µsec (1024 clocks @ 40MHz), whichever comes first.

ADC0 Data: Word32 Offset 0x0000

Reading this register returns ADC0 data. ADC0 reads the difference between the Channel 0 output (after analog summer) and the power supply 0 feedback input.

ADC0 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC0 Data (-32768 – 32767 = -10V to 10V)

ADC1 Data: Word32 Offset 0x0001

Reading this register returns ADC1 data. ADC1 reads the difference between the Channel 1 output (after analog summer) and the power supply 1 feedback input.

ADC1 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC1 Data (-32768 – 32767 = -10V to 10V)

ADC2 Data: Word32 Offset 0x0002

Reading this register returns ADC2 data. ADC2 reads the difference between the Channel 2 output (after analog summer) and the power supply 2 feedback input.

ADC2 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC2 Data (-32768 – 32767 = -10V to 10V)

ADC3 Data: Word32 Offset 0x0003

Reading this register returns ADC3 data. ADC3 reads the difference between the Channel 3 output (after analog summer) and the power supply 3 feedback input.

ADC3 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC3 Data (-32768 – 32767 = -10V to 10V)

Channel 0 Tolerance: Word32 Offset 0x0004

Sets or returns the Channel 0 tolerance.

If the absolute value of the ADC0 reading is greater than the Channel 0 Tolerance for sixteen consecutive samples, Channel 0 is declared “out of tolerance” and the Channel 0 Out Of Tolerance bit will be set.

Channel 0 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 0 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 1 Tolerance: Word32 Offset 0x0005

Sets or returns the Channel 1 tolerance.

If the absolute value of the ADC1 reading is greater than the Channel 1 Tolerance for sixteen consecutive samples, Channel 1 is declared “out of tolerance” and the Channel 1 Out Of Tolerance bit will be set.

Channel 1 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 1 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 2 Tolerance: Word32 Offset 0x0006

Sets or returns the Channel 2 tolerance.

If the absolute value of the ADC2 reading is greater than the Channel 2 Tolerance for sixteen consecutive samples, Channel 2 is declared “out of tolerance” and the Channel 2 Out Of Tolerance bit will be set.

Channel 2 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 2 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 3 Tolerance: Word32 Offset 0x0007

Sets or returns the Channel 3 tolerance.

If the absolute value of the ADC3 reading is greater than the Channel 3 Tolerance for sixteen consecutive samples, Channel 3 is declared “out of tolerance” and the Channel 3 Out Of Tolerance bit will be set.

Channel 3 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 3 Tolerance (-32768 – 32767 = -10V to 10V)

ADC Status: Word32 Offset 0x0008

Reading this register returns the Out Of Tolerance bits for all four channels. Writing 0 to a set bit will clear it.

ADC Status

Bits	Bit Definitions
31:4	Reserved
3	Channel 3 Out Of Tolerance 1 = Out Of Tolerance
2	Channel 2 Out Of Tolerance 1 = Out Of Tolerance
1	Channel 1 Out Of Tolerance 1 = Out Of Tolerance
0	Channel 0 Out Of Tolerance 1 = Out Of Tolerance

6. Front Panel LEDs

The front panel LEDs are mapped to LED_DATA_0_BASE. Writing 0 to any of these bits will turn that LED on.

Front Panel LEDs

Bits	Bit Definitions
31:8	Reserved
7	Heartbeat
6	Ramp 0 Enabled
5	Ramp 1 Enabled
4	Ramp 2 Enabled
3	Ramp 3 Enabled
2	PS Interlock (Logical AND of all 4 interlocks)
1	Reserved for MDAT Present
0	TCLK Present

7. Power Supply Status
The 32 digital power supply status inputs (4 channels x 8 bits) are read here. Power supply status is mapped to PS_STATUS_0_BASE.

Power Supply Status

Bits	Bit Definitions
31:24	Power Supply 3 Status
23:16	Power Supply 2 Status
15:8	Power Supply 1 Status
7:0	Power Supply 0 Status

8. CAMAC Interface
The CAMAC interface is mapped to CAMAC_IF_OFFCHIP_0_BASE.

Read CAMAC R[16:1]: Word32 offset 0x0000 (Read)
Reading address offset 0x0000 will capture data from the CAMAC R bus (R[16:1]). Reading this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
31:16	Reserved
15:0	CAMAC R[16:1]

Set CAMAC W[16:1]: Word32 offset 0x0000 (Write)
Writing address offset 0x0000 will set data on the CAMAC W bus (W[16:1]). Writing this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
31:16	Reserved
15:0	CAMAC W[16:1]

Capture Function and Subaddress (F/A): Word32 offset 0x0002 (Read)
Reading address offset 0x0002 will capture the state of the F and A CAMAC dataway signals. Reading this address will clear the CAMAC Interface interrupt for Functions 9 – 31. Reading this address will have no effect on the state of the CAMAC Interface interrupt for Functions 0 – 8.

Bits	Bit Definitions
31:9	Reserved
8	F16
7	F8
6	F4
5	F2
4	F1
3	A8
2	A4
1	A2
0	A1

Clear Invalid Interrupt: Word32 offset 0x0002 (Write)
Writing address offset 0x0002 will clear the CAMAC interrupt, and no Q will be sent back to the CAMAC controller. Use this to clear an interrupt if an invalid Function or Subaddress is given, or if any other error occurs that does not allow the system to complete the CAMAC command.

Bits	Bit Definitions
31:0	Unused. Data will be ignored.

Set/Clear Look-At-Me (LAM): Word32 offset 0x0003 (Write)
Writing address offset 0x0003 will set the LAM CAMAC Dataway signal.

Bits	Bit Definitions
31:2	Unused. Data will be ignored.
1	LAM Mask 1 = Enable LAM 0 = Disable LAM
0	Logic state to set LAM to 1 = TRUE (Low) 0 = FALSE (High)

9. FPGA Version (FPGA_VERSION.VHD)
The FPGA version is contained in a small module dedicated to this purpose only. The module is mapped to FPGA_VERSION_0_BASE.

FPGA Version

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision